A New design using CLRCL Full Adder Logic in 180 nm Technology

Keshav Kumar, Amit Grover

Abstract— This article explains a low complexity full adder design using 10 transistors having higher computing speed, lower operating voltage and lower energy consumption. The simulation results, based on 0.18um process models indicate that the proposed de sign has the lowest working **Vdd** and highest working frequency. Apart from this, the performance edge of the proposed design in terms of speed and energy consumption become even more significant as the word length of the adder increases.

Keywords— Complementary & Level Restoring Full Adder, Boolean Logic

1 INTRODUCTION

THIS essence of the digital computing lies in the full adder design. The design criteria of a full adder are usually multifold. Numerous full adder designs in the categories of fully static CMOS, dynamic circuit, transmission gate or pass transistor logic have been presented. Transmission gate plus inverter based full adder designs [1] were presented using 20 and 16 transistors. Usage of pass transistor logic in lieu of transmission gate reduces the transistor count. Full adder design [2] consists of only 14 transistors along with pass transistor logic based XOR/XNOR circuits. Despite the saving in transistor count, the output voltage level is degraded at certain input combinations due to threshold voltage loss problem. At the cost of two additional transistors, the design was further improved in [3] and can eliminate the inverter from the critical path to avoid the possible short circuit power consumption for low power operation. In [4], a pass transistor based new Static Energy-Recovery Full (SERF) adder with as few as 10 transistors was presented. In [5], improved 10-transistor full adder designs were derived based on systematic exploration of the combinations of various XOR, sum and carry out modules. In [6], another 10-transistor full adder design consisting of two pass transistor based XORs and a 2-to-1 multiplexer was presented. In this article, we will propose a novel 10-transistor full adder design with alleviated threshold loss problem.The design can also sustain lower Vdd operation than peer designs.

The major sources of power consumption in digital CMOS circuits are summarized in the following equation**.**

$$P_{total} = P_{switching} + P_{short\text{-}circuit} + P_{leakage}$$

$$= (\alpha_{0\to1} \times C_L \times V_{dd}^2 \times f_{clk}) + (I_{sc} \times V_{dd}) + (I_{leakage} \times V_{dd})$$

The first term represents the switching component of power, where C is the load capacitance, f_{clk} is the clock frequency and $\alpha_{0\to1}$ is the node transition activity factor. The second term is due to the direct path short circuit currents, I_{sc}, which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current, $I_{leakage}$, which can arise from substrate injection and sub threshold effects, is primarily determined by fabrication technology considerations.

2 THE PROPOSED CLRCL FULL ADDER DESIGN

The logic function of a full adder can be represented as

$$Sum = (A \odot B)\cdot Cin + (A \oplus B)\cdot \overline{Cin} \quad (1)$$

$$Cout = (A \oplus B)\cdot Cin + (A \odot B)\cdot A \quad (2)$$

From Eq (1) and (2), we can easily identify two basic modules needed in implementing the functions, i.e. XOR and 2-to-1 multiplexer. An XOR/XNOR function can be achieved with only 4 transistors in pass transistor logic. In this paper, we propose a novel full adder design featuring Complementary and Level Restoring Carry Logic (CLRCL). The goal is to reduce the circuit complexity and to achieve faster cascade operation. Figure 1 shows the circuit diagram of 10-T Complementary & Level Restoring Full adder.

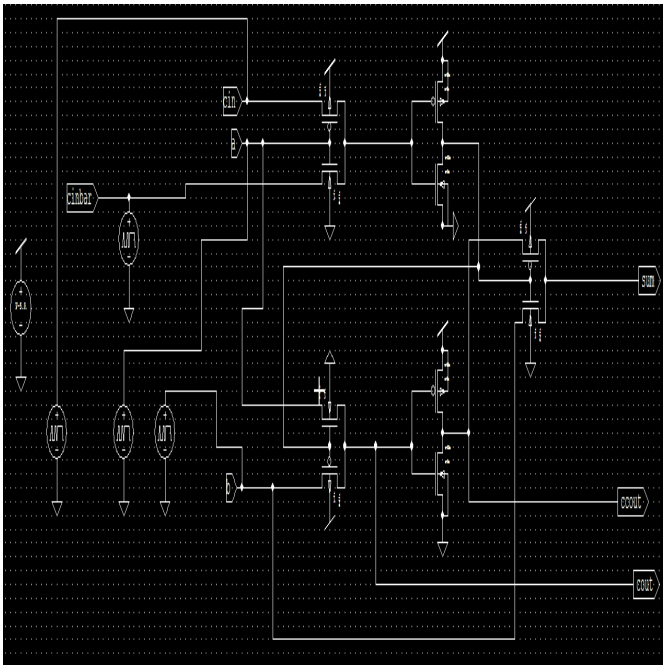


Fig.1. Circuit Diagram of 10-T Complementary & Level Restoring Full Adder

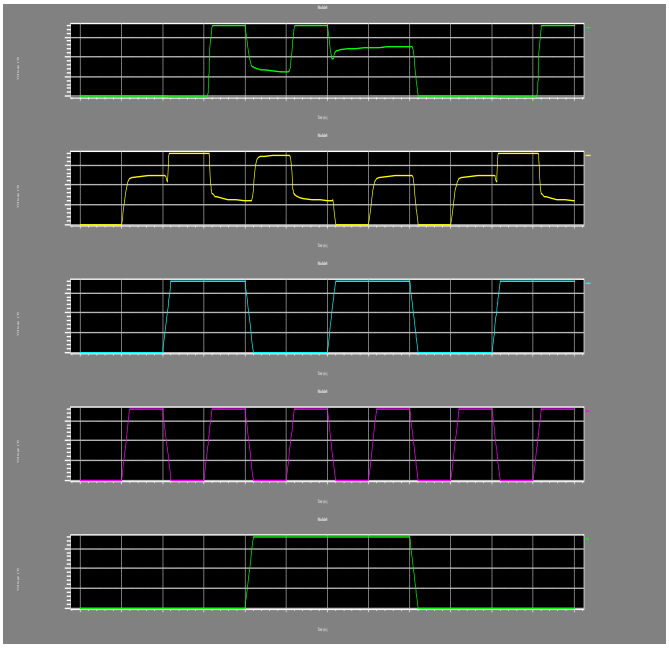
Fig.2. Waveform of 10-T Complementary & Level Restoring Full Adder

3 Final Results

The result of 10-T is carried out at 1.2v, 1.5v, 1.8v supply voltages. The different parameters like average powers consumed, delay at sum and carry output have been found as mentioned in table 1. Figure 2 shows the waveform of carry select adder at sum output and at carry output.

Table 1
Parameters of 10T Complementary & Level Restoring Full Adder

Design Style	Voltage	No. of transistors	Minimum Length (μm)	Avg. Power Consm. (watts)	Prop. Delay at Sum (sec)	Prop. Delay at carry(sec)
FA	1.2	10	.18	$1.55*10^{-4}$	$4.96*10^{-10}$	$6.34*10^{-9}$
FA	1.5	10	.18	$6.82*10^{-6}$	$6.30*10^{-10}$	$1.08*10^{-7}$
FA	1.8	10	.18	$1.51*10^{-5}$	$7.68*10^{-10}$	$1.08*10^{-7}$



4 Conclusion

This article explains complementary & level restoring full adder using 10 transistors. The results have been carried out at different voltages of 1.2, 1.5 and 1.8 V. The circuit consumes lesser power at 1.5 V as compare to 1.2 & 1.8 V. In 10-T circuit delay at carry output is high when we use 1.5 & 1.8 V and lesser delay is carried at sum output at 1.2 V. So, it has been concluded that, when we use 10-T circuit then it consumes less power but delay in this increases.

References

[1] N. Zhuang and H. Wu, "A new design of the CMOS full adder,"
IEEE J. of Solid state circuits, Vol. 27, pp. 840-844, May 1992.

[2] J. Wang, S. Fang, and W. Feng, "New efficient designs for XOR and XNOR functions on the transistor level," IEEE J. Solid-State Circuits, vol. 29, pp. 780-786, July 1994.

[3] A. M. Shams and Magdy A. Bayoumi, "A Novel High-Performance CMOS 1-Bit Full Adder Cell," *IEEE Trans. Circuits and Systems-II*, Vol.47 No.5, May 2000.

[4] R. Shalem, E. John, and L. K. John, "A novel low-power energy recovery full adder cell," in *Proc. Great Lakes Symp. VLSI*, pp. 380—383, Feb. 1999.

[5] H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power 10- transistor full adders using novel XOR-XNOR gates," *IEEE Trans. On Ckt and Systems II*, Vol. 49, no.1, PP.25 — 30, Jan 2002.

[6] A. Fayed and M. Bayoumi, "A low power 10-transistor full adder cell for embedded architectures,"/EEE *Symposium of Circuits and Systems, Sydney, Australia*, pp.226 -229, May 2001.

Author's Biography

Keshav Kumar is pursuing his Master of Technology in the area of Electronics and Communication Engineering under the supervision of Mr. Amit Grover, Assistant Professor, Department of Electronics and CommunicationEngineering, Shaheed Bhagat Singh State Technical Campus (Established by Govt. of Punjab) Moga road, Ferozepur, Punjab, India. The author place of birth is Banmankhi, Distt. Purnea, Bihar India on 15th, April 1989. Keshav Kumar received his B. Tech degree in the area of Electronics & Communication Engineering in 2011 From Baba Hira Singh Bhattal Instituteof Engineering & Technology (Established by Govt. of Punjab) Lehragaga, Distt-Sangrur, Punjab, India. His areaof interest includes Signal processing, MIMO systems, Wireless mobile communications, High speed digital communications and 4G Wireless

communications.

Amit Grover became a Member (M) of Association ISTE in 2006, a Senior Member (SM) of society SELCOME in September 2009, and a Project-In charge (PI) in august 2011 and in September 2012. The author place of birth is Ferozepur, Punjab, India on 27th, September 1980. The author received his M. Tech degree in Electronics and Communication Engineering from Punjab Technical University, Kapurthla, Punjab, India in 2008 and received his B. Tech degree in Electronics and Communication Engineering from Punjab Technical University, Kapurthala, Punjab, India in 2001. Currently, he is working as an Assistant Professor in Shaheed Bhagat Singh State Technical Campus, Ferozpur, Punjab, India. His area of interest includes signal processing, MIMO systems, Wireless mobile communications, High speed digital communications, 4G Wireless communications and VLSI Design.